BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

Paragraphs beginning on Page 1, lines 6 and 18:

In order to reduce the size of semiconductor devices numerous techniques have been developed to vertically stack one semiconductor die, hereinafter "die", on top of another die. Figure 1 illustrates a conventional method of vertically stacking two die 20, 30 on a support structure 10, such as a printed circuit board (PCB) or other thin support structure, to form a conventional semiconductor assembly 100. The first die 20 is shown secured to a support structure 10 by an adhesive material 22_a using techniques well known in the art. When the first die 20 is pressed against the support structure 10 the adhesive material 22_a is partially forced outside the die's 20 perimeter 29 and forms an adhesive fillet 24_a. Likewise, when the second die 30 is secured against the first die 20 by an adhesive material 22_b a second adhesive fillet 24_b is also formed.

A1

Both the first die 20 and second die 30 are shown wire bonded 40 to an electrical contact area 18 on the support structure 10. The first die 20 has an electrical contact area 28, such as a bonding pad, on its top surface 26. Because adhesive fillet 24_b is formed when the second die 30 is secured to the first die 20, it limits the placement of the first die's 20 electrical contact area 28. The distance B between the perimeter 39 of the second die 30 and a first die's 20 electrical contact area 28 must be increased by distance A, the width of the adhesive fillet 24_b, to provide sufficient operating space for the wire bonding equipment. Typical dimensions for distances B are about 428 microns or greater to allow for adhesive fillets 24_b, which are conventionally about 228 microns in width or greater. Using current wire bonding equipment, distance B between electrical contact area 28 and the perimeter of the fillet 24_b can be reduced to about 200 microns or less. In

A2

other words, adhesive fillet 24_b requires about 228 microns or more of first die's 20 top surface 26 on each side of the first die 20. If the adhesive fillet 24_b were eliminated the space could be used either to increase the size of the second die 30 or to reduce the size of the first die 20.

A2

Cancluded

Paragraph beginning on Page 5, line 15:

Referring now to the drawings, where like elements are designated by like reference numerals, Figures 2-3, illustrate a plan and elevation view respectively of a partially completed semiconductor assembly 200 in which a first semiconductor die 20 is secured to the top surface 16 of supporting structure 10, by a first adhesive layer 22_a. Supporting structure 10 in an exemplary embodiment is a printed circuit board or thin film, but may be any structure suitable for supporting a semiconductor die. The supporting structure 10 is shown as having two electrical contact areas 17 on surface 16 and the first die 20 is also shown as having two electrical contact areas 28. It is to be understood that any number of electrical contact areas 17, 28 may be provided on the support structure 10 and first die 20. Also, although Figure 2 shows the contact areas 17, 28 as recessed, they may also be formed on the surface of the support structure 10 or first die 20, respectively, and could be electrically connected to external electrical paths or to other parts of the completed semiconductor assembly 200.

A3

Paragraph beginning on Page 6, line 10:

A second adhesive layer 22_b is shown in Figure 2 as deposited on a top surface 26 of the first semiconductor die 20 within an adhesive layer area defined by a perimeter 34. The second adhesive layer 22_b can be deposited by techniques well-known in the art to include various patterns and coverage areas. It is to be understood that perimeter 34 is representative of an area of deposition of the second adhesive layer 22_b; however it is not limiting. In accordance with the invention a sufficient amount of adhesive material should be deposited to adequately secure a second semiconductor die 30 (see Figures 4-5) to the first semiconductor die 20. The invention includes any coverage area or pattern that does not exceed the perimeter of the second die 30. As described below, when the second die 30 is placed and pressed on the first die 20, the adhesive layer 22_b represented inside of the adhesive perimeter 34 does not extend past the profile or perimeter 39 of the second die 30 (Figures 4-5).

Paragraphs beginning on Page 7, lines 4 and 14:

Figures 4-5 show the assembly 200 after a second die 30 with electrical contact areas 38 on the die's top surface 36 is pressed against the second adhesive layer 22_b located on the top surface 26 of the first die 20. A cavity 25 is formed between the dies 20 and 30 and is characterized by a distance D between the perimeter 34 of the second adhesive layer 22_b and the perimeter 39 of the second die 30. The distance D may be a regular or irregular distance around the periphery of the adhesive layer 22_b. It is to be understood

that formation of cavity 25 is not essential, what is important is that adhesive layer 22_b does not extend beyond the perimeter 39 of the second die 30 such that no adhesive fillet 24 is formed.

If cavity 25 is present, the distance D is preferably in the range such that between about 50 and about 90 percent of the second die 30 bottom surface is covered by the second adhesive material layer 22_b. Figures 4 and 5 show distance C between the perimeter 39 of the second die 30 and the perimeter 29 of the first die 20. This distance is a value which provides acceptable clearance between electrical contact area 28 and the second die 30 to enable the formation of electrical contacts between the dies 20, 30 and other parts of the assembly 200 such as wire bonds 40 between the dies 20, 30 and the support structure 10 (Figure 6). An exemplary distance C between the perimeters 29, 39 of the first die 20 and second die 30 is about 200 microns or less. The distance C is currently only limited by the technology of the wire bond equipment and the minimum required operating space.

Paragraph beginning on Page 8, line 16:

Also shown are balls 60 which make up a ball grid array pattern for making electrical connections between the support structure 10 and external electrical circuits. The balls 60 are deposited on the support structure 10 using materials and techniques well known in the art and are electrically connected through conductors supported by support structure 10 to the contact areas 17. It is to be understood that multiple semiconductor

assemblies 200 could be prepared at one time on a continuous support structure 10, which could be separated into individual or multiple semiconductor assemblies 200 at a later stage of fabrication.

Paragraphs beginning on Page 9, lines 4 and 12:

Figure 6 also shows an encapsulating material 50, such as a molding compound, deposited over the wire bonds 40, semiconductor dies 20, 30, and top surface 16 of the support structure 10. As an exemplary illustration, some of the encapsulation material 50 is shown under the second die 30 and within cavity 25 (Figures 4-5) and provides support and stability to the second die 30. The encapsulating material 50 and molding techniques using it are well known in the art and not repeated herein.

Figure 7 is a cross-sectional illustration of a second exemplary embodiment of a semiconductor assembly 300 with second and third semiconductor dies 30, 45 secured to a first semiconductor die 20 using the techniques described above. It is to be understood that the elimination of the adhesive fillet 24_b as discussed in Figure 1 covers a wide range of semiconductor configurations involving multiple dies with various sizes, dimensions, and electrical contact techniques. The above described invention has the advantage of allowing either the size of the second and third semiconductor dies 30, 45 to be increased or allowing the size of the first semiconductor die 20 to be reduced by eliminating the wasted space occupied by the adhesive fillet 24_b.